In the Specification:

Please amend the paragraph beginning at page 12, lines 11-22 as indicated below:

Figure 1E illustrates removal of the mask **30** and formation of the ohmic contacts **40** in the recesses **41** defined by (i.e., adjacent) the second cap layer **24**. The ohmic contacts **40** may be fabricated as described in U.S. Patent No. 6,316,793. The ohmic contacts **40** are formed on the first cap layer **22**. The ohmic contacts **40** on the first cap layer **22** may be annealed at a relatively low anneal temperature. For example, in certain embodiments of the present invention, anneal temperatures of from about 400 to about 800 °C may be used. In other embodiments of the present invention the anneal step may be eliminated. Thus, the ohmic contacts **40** may be provided without the need for high anneal temperatures or to etch the Group III-nitride materials of a cap layer. The transistor may be further completed by addition of a gate 28 and/or gate structure, passivation or other such additional processing as known to those of skill in the art.

Please amend the paragraph beginning at page 13, lines 21-29 as indicated below:

The second cap layer **24'** is selectively grown utilizing a mask as described above as a doped AlGaN layer, intentionally or otherwise, with an Al concentration of about 20% and doped with an n-type dopant such as Si to a concentration of about 2×10^{12} cm^{-2} total. The second cap layer **24'** may have a thickness of about 10 nm. An additional layer **26'** is selectively grown utilizing a mask as described above as an undoped AlGaN with an Al concentration of about 20% is also provided on the second cap layer **24'**. The additional layer **26'** may have a thickness of about 10 nm. Ohmic contacts **40** are formed in the recesses **41'** adjacent the second cap layer **24'** and the additional layer **26'**. A gate contact **28'** may be formed on the additional layer **26'**.

Please amend the paragraph beginning at page 14, lines 1-5 as indicated below:

The second cap layer **24''** is selectively grown utilizing a mask as described above as an undoped AlGaN layer with an Al concentration of about 20%. The second cap layer **24''** may have a thickness of about 20 nm. Ohmic contacts **40** are formed in the recesses **41''** adjacent the second cap layer **24''**. A gate contact **28''** may be formed on the second cap layer **24''**.

Please amend the paragraph beginning at page 15, lines 12-22 as indicated below:

The second cap layer **24'''** is selectively grown utilizing a mask as described above except the mask is used to mask the gate region of the device. The second cap layer **24'''** may be an undoped AlGaN layer with an Al concentration of about 20%. The second cap layer **24'''** may have a thickness of about 5 nm. An additional layer **26''** is selectively grown utilizing a mask as described above as a doped AlGaN layer doped n+, for example, doped to a carrier concentration of from about 10^{18} to about 10^{20} cm^{-3}. The additional layer **26''** may have an Al concentration of about 20%. The additional layer **26''** may have a thickness of about 10 nm. Ohmic contacts **40'** are formed on the additional layer **26''**. A gate contact **42** may be formed on the first cap layer **22'''** in the recess **41'''** formed by the second cap layer **24'''** and the additional layer **26''**.

Please amend the paragraph beginning at page 14, lines 23-31 as indicated below:

Figure 5 shows a transistor according to further exemplary embodiments of the present invention, in which gate and ohmic contacts are both formed in regrown recesses. A channel layer **520** and a first cap layer **522** may be formed on a substrate **510** as described above (it will be appreciated that the substrate **510** may include buffer layers and/or other layers). The first cap layer **522** may be masked to expose portions of the first cap layer **522**, and second cap layers **524** may be formed on the exposed portions. The mask may then be removed to leave recesses **541** adjacent the second cap layers **524**. Ohmic and gate contacts **540** and **528** may be formed in the recesses **541**, as shown.

Please amend the paragraph beginning at page 14, line 32 through page 15, line 10 as indicated below:

Figure 6 shows a transistor according to other exemplary embodiments of the present invention, in which gate and ohmic contacts are both formed in regrown recesses, but on different nitride-based layers. A channel layer **620** and a first cap layer **622** may be formed on a substrate **610** as described above (it will be appreciated that the substrate **610** may include buffer layers and/or other layers). The first cap layer **622** may be masked to expose a portion of the first cap layer **622**. A second cap layer **624** may then be formed on the exposed portion. An additional mask may then be formed on the second cap layer **624**, leaving spaced apart portions of the second cap layer exposed. Additional layers **626** may be formed on these exposed portions. The masks may be removed to leave recesses **641** that expose first and second portions of the first cap layer **622** and a portion of the second cap layer **624**. Ohmic and gate contacts **640** and **628** may be formed in the recesses **641**, as shown. It will be appreciated that the order of masking and contact formation operations may be varied.